Video-SCSI/HP-IB Board

Important Note

The SCSI option will not be available at SPU introduction but will be delayed for several months. Contact your local HP Sales and Service Office for more information.

Depending on the option ordered, this board will have the following functions as listed below and pictured in Figure 3-9.

- Only video circuits, 98564-66570.
- Video and SCSI circuits, 98564-66571.
- Video and high-speed HP-IB, 98564-66572.

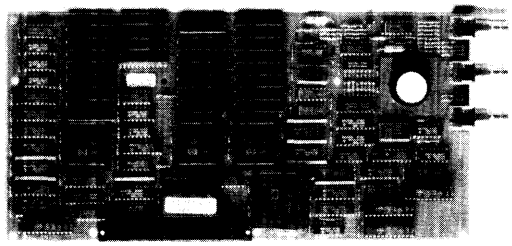

Figure 3-9a. Video Board with Video Circuits

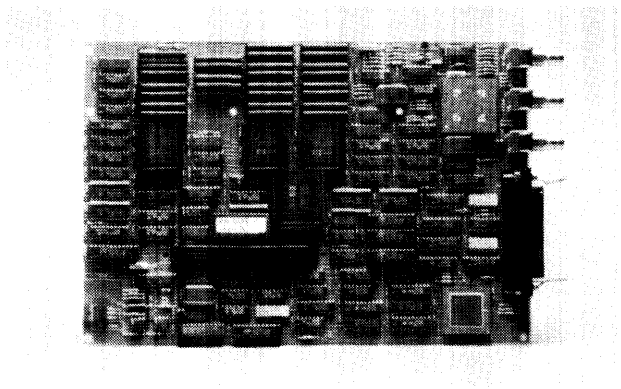

Figure 3-9b. Video Board with Video and SCSI Circuits

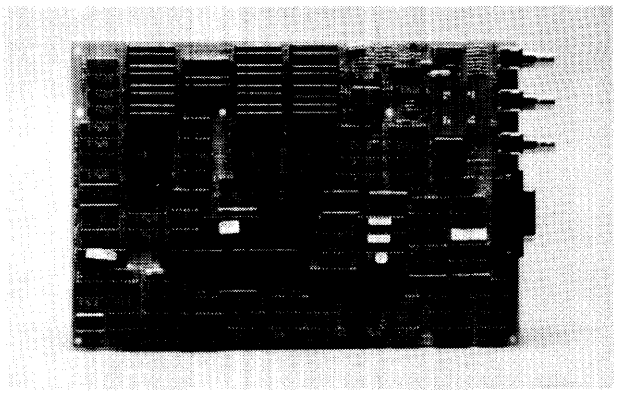

Figure 3-9c. Video Board with Video and High-Speed HP-IB Circuits

Video Circuit

Overview

Video circuits provide high-resolution color video for color monitors. Resolution is 1024 by 768 pixels from a 6-plane frame buffer.

Software compatible with previous 4 and 6 plane video boards with HP-UX operating system can also be used with the Model 319C+ Workstation.

A hardware cursor isn't used, therefore the flashing underscore cursor is not available on the video. It is implemented by software.

The Bit-Blt (bit-boundary block transfer) functions of the video are greatly improved over previous video boards in that bit per pixel operations are supported as well as previous byte per pixel.

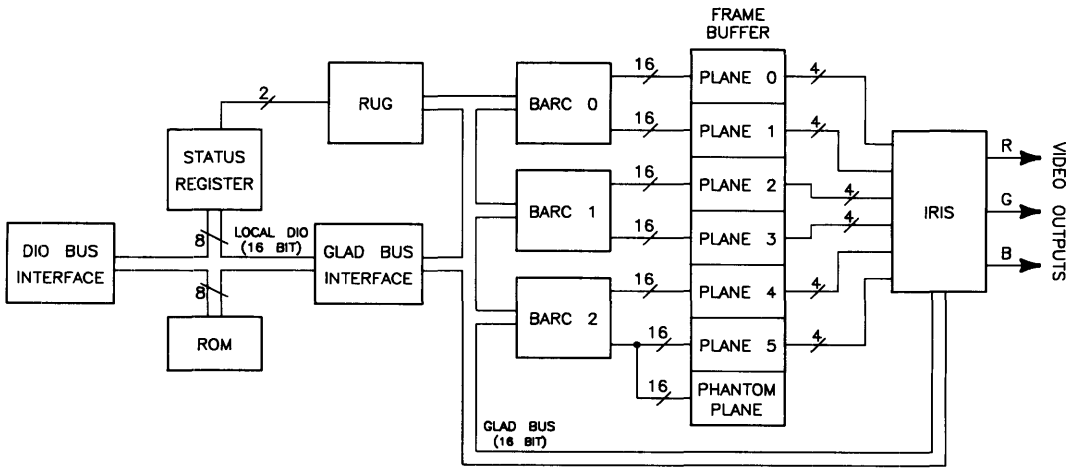

Figure 3-10. Video Circuit Block Diagram

Functional Description

GLAD Bus Controller. The GLAD (Graphics Logical Address and Data) bus control signals are generated by several on-board PALs. The controller arbitrates between cycle requests for:

- VRAM shift register data transfer and refresh.
- Scan Converter vector/Bit-Blt read/write operations.
- SPU frame buffer/register read/write operations.
- All VRAM refresh.
- Read/write cycles to and from VRAM.
- Read/write cycles to and from registers in the Scan Converter, BARC (Bi-planer Access RAM Controller), and IRIS (color map and video controller chip).

GLAD Bus. The GLAD bus is a 16-bit multiplexed address and data bus designed for tightly coupled communication between Scan Converter, BARC, IRIS, and the frame buffer (throught BARC).

Scan Conversion. The Scan Converter chip generates and clips pixels. Given vector end points, it performs the Bresenham algorithms to produce the individual pixel addresses which it then writes to the frame buffer through the BARC data path chips (one BARC for every two planes of frame buffer).

It also has circuits to make circles and area filling. For circles, the center point and radius are written to the Scan Converter which generates and clips the pixels. The area fill is accomplished by a triangle fill algorithm where the CPU provides pre-sorted polygon vertices. These triangles are filled into a phantom plane.

Both 2 and 3 operand Bit-Blt functions are supported. The 2 operand Bit-Blt is controlled by the window replacement rule. The 3 operand Bit-Blt is controlled by the three operand replacement rule. The BARC chips control the type of Bit-Blt being performed.

Color Mapping and Display Control. The IRIS chip controls the serial ports of the VRAM and converts all the data stream from the VRAMs to the appropriate color as defined by the color lookup table in IRIS. IRIS has 8 bit DACs driving the output. With 6 planes, 64 colors are displayable at any one time. All of the video control signal generation is provided by IRIS. These signals are combined with the data stream inside IRIS so the RGB video outputs are taken directly from the IRIS output pins.

ID/Font ROM. The ID/Font ROM provides the CPU information about the video circuits. Pixel matrix, initialization, and dot clock frequency data is provided. The ROM is a 256K ROM that has the first 8 Kwords, accessible 1 byte at a time on odd byte boundaries, and the last 16 Kwords used for display ID ROM functions.

Alpha character font is the size and shape of the dot matrix for creating alpha characters. The system monitor displays the font required for the application, and opreating system. Sometimes the software will specify another available font to be used if required. Standard pixel display matrix is a 6 by 10 character matrix in an 8 by 16 character cell.