OTI-077
Extended High Resolution VGA Graphics Controller with 1MByte Video Memory Support

DESCRIPTION

The OTI-077 is a highly integrated, single chip Extended High Resolution VGA Graphics Controller compatible with the IBM VGA standard. The package dimensions and pin count are identical to the OTI-067. However, enhancements have been made to the OTI-077 to increase functionality. In addition to the Oak Technology extended VGA modes implemented in the OTI-067, the OTI-077 provides a high resolution of 1024x768 with 256 colors and 1280x1024 with 16 colors. The OTI-077 is completely compatible with the IBM VGA standard and implements all registers, and data paths while providing improved performance and additional functionality. It is backwards compatible with EGA/CGA/ MDA and Hercules graphics modes. Especially attractive for motherboard applications is the low external chip count which can be achieved by using Oak's proprietary highly integrated VGA controller which supports 256K X 4 DRAMs. Application notes for using the OTI-077 in a motherboard implementation are available by contacting Oak Technology.

FEATURES

- Supports up to 1MByte of video memory.
- Extended resolutions up to 640x480, 32K colors; 1024x768, 256 colors; and 1280x1024, 16 colors.
- Supports VESA - standard high vertical refresh rates of 72 Hz for flicker-free displays.
- VGA, EGA, CGA, MDA and Hercules compatible.
- Pin compatible with the OTI-067.
- Compatible with OTI-067 drivers for 640x480, 256 color mode; 800x600, 16 and 256 color modes; and 1024x768, 16 color mode.

SOFTWARE DRIVER SUPPORT

Oak Technology realizes the importance of the hardware-software driver relationship. We are committed to providing our customers with the most powerful software drivers. Our software driver support includes some of the fastest drivers available for popular applications including:

AutoCAD
AutoShade
CADvance
GEM
Lotus 1-2-3
Microsoft Windows
P-CAD
Presentation Manager
Ventura
VersaCAD
VESA BIOS Extensions
WordPerfect
Wordstar

In addition to these OTI-067 drivers, software driver support has been expanded for the OTI-077 to include support for Microsoft Windows in 640x480 32K color mode, 1024x768 256 color mode and 1280x1024 16 color mode. Software driver support for AutoCAD has also been expanded to include 1024x768 256 color mode and 1280x1024 16 color mode.

RESOLUTION, COLOR AND MONITOR SUPPORT

Resolution	Colors	Max Vertical Refresh	Group I	Group II	Group III	Group IV	Group V	VESA Compliant
320x200	16,256	70 Hz	X	X	X	X	X	N/A
512x512	32K	56 Hz				X	X	N/A
640x400	32K	56 Hz				X	X	N/A
640x480	32K	56 Hz				X	X	N/A
640x480	16,256	60 Hz	X	X	X	X	X	X
640x480	16,256	72 Hz			X	X	X	X
768x1024	16	60 Hz					X	X
800x600	16,256	56 Hz		X	X	X	X	X
800x600	16,256	60 Hz		X	X	X	X	X
800x600	16	72 Hz				X	X	X
1024x768	4,16	60 Hz				X	X	X
1024x768	16,256*	87 Hz					X	X
1024x768	16	72 Hz					X	N/A
1280x1024*	16	87 Hz					X	N/A

* Interlaced mode

Monitor Definitions

Category	Type	Vertical Frequency	Horizontal Frequency	Notes
Group I	VGA	60 & 70 Hz	31.5 KHz	Basic VGA
Group II	SVGA	56,60,70 Hz	31.5 & 35 KHz	NEC 2A Type
Group III	Multi-Frequency	50 to 90 Hz	15.75 to 38 KHz	NEC 3D Type
Group IV	Multi-Frequency	50 to 90 Hz	30 to 57 KHz	NEC 4D Type
Group V	Multi-Frequency	50 to 90 Hz	30 to 66 KHz	NEC 5D Type

PIN DIAGRAM

The Pin Diagram for the OTI-077 is identical to that of the OTI-067 shown on page 6 of the OTI-067 databook.

SYSTEM BLOCK DIAGRAM

The System Block Diagram for the OTI-077 is identical to that of the OTI-067 shown on page 7 of the OTI-067 data book.

OTI-077 INTERFACES

The BIOS ROM Interface, Clock Interface and Video Interface are identical to those of the OTI-067 shown on pages 8 and 9 of the OTI-067 data book.

CPU Interface

The CPU interface for the OTI-077 is identical to that used in the OTI-067 for add-on card implementations. For information regarding the CPU interface for motherboard implementations using the OTI-077 consult the OTI-077 application notes.

DRAM Interface

The OTI-077 supports 256K X 4 DRAM ICs in all modes. It supports 256 KBytes of video memory by using two 256 X 4 DRAM chips; 512KBytes of video memory by using four 256K X 4 DRAM chips and 1MByte of video memory by using eight 256K X 4 DRAM chips. The OTI-077 provides the same control signals and address/data lines to the video memory in page mode as the OTI-067. For a 44 MHz memory clock, DRAMS with an access speed of 80ns are required, 70ns DRAMs are required for a 50 MHz memory clock, the same as with the OTI-067.

In extended modes with 256 colors, the video memory is organized in a packed pixel mode; 1 byte per pixel. This requires programming of an OTI extended register and may use either 512 KBytes or 1 MByte of DRAM depending on the resolution. For 16 color extended modes, the video memory is organized as planar mode (1 bit from each of 4 planes) which is compatible with IBM's 16 color graphics mode.

FUNCTIONAL DESCRIPTIONS

The six major functional blocks of the OTI-077 are

1- CRT Controller (CRTC)
2-Attribute controller
3-Graphics controller
4-Sequencer
5-Memory buffer
6-Bus interface

The functional descriptions for the six major functional blocks of the OTI-077 are identical to those of the OTI-067.

PIN DESCRIPTIONS

Most pin descriptions for OTI-077 are identical to those found on pages 13-15 of the OTI-067 databook. The following pin name/description changes are applicable when taking advantage of the new features of the OTI-077.

RDSWn (108)-Read Dip Switch. This is a dual function pin (RDSWn/CAS2n). It is dependent on the configuration register 3DF index 12 bit 3 (pin CSEL0). In OTI-077 configurations it is used to set the second 512K bytes of video memory for use in 1 MByte configurations.

3DFix12b3:2=0	RDSWn
3DFix12b3:2=1	CAS2n

There is no penalty in setting this pin to an active (high) position when used in configurations having only 512K bytes of video memory.

ROMENLn (63)-ROM Low Byte Enable. This pin is used to control the BIOS ROM when implementing an add-on card configuration. When using a motherboard implementation this pin is not used. The OTI-077 uses this pin in a dual role (ROMENLn/ALE) depending on the configuration register 3DF index 12 bits 2&3.

3DFix12b3:2=00	ROMENLn
3DFix12b3:2=01	ROMENLn
3DFix12b3:2=10	ROMENLn
3DFix12b3:2=11	ALE

Pin ALE is used to latch in the decode of LA23-LA20 for complete 24 bit address decode when in an on-board configuration. However, this latch will be opened when in Master mode (because the Master device does not generate ALE) or by RA12.

RA12(64)-ROM address bit 12. This pin serves different purposes for OTI-067 and OTI-077 configurations:

For OTI-067 Implementations
1- ROM address bit 12. This pin is used if ROM paging is desired.
2-Configuration pin bit 0. This function is only active during hardware reset (RSET is high).

For OTI-077 Implementations
1- ROM address bit 12. This pin is used if ROM paging is desired.
2- DMA Hold Acknowledge(HLDA). RA12 becomes HLDA in on-board configurations(this condition is similar to those necessary to activate ALE). HLDA is needed along with AEN and RFSHn to differentiate between CPU mode, Master mode and DMA mode.

See OTI OVERFLOW REGISTER II pages 5-6.

SUPPORTED SCREEN FORMATS

The OTI-077 provides support for all IBM standard VGA modes.

The OTI-077 supports the following OTI Extended Modes:

Mode	Colors	Rows	Char Cell	Display Mode	Resolution	Buffer Start	#DRAMs	Non/Interlaced
4E	16	80x60	8x8	Text	640x480	B8000	2/4/8	Non-Interlaced
4F	16	132x60	8x8	Text	1056x480	B8000	2/4/8	Non-Interlaced
50	16	132x25	8x14	Text	1056x350	B8000	2/4/8	Non-Interlaced
51	16	132x43	8x8	Text	1056x344	B8000	2/4/8	Non-Interlaced
52	16	100x37.5	8x16	Graphics	800x600	A0000	2/4/8	Non-Interlaced
53	256	80x30	8x16	Graphics	640x480	A0000	4/8	Non-Interlaced
54	256	100x37.5	8x16	Graphics	800x600	A0000	4/8	Non-Interlaced
55	4	128x48	8x16	Graphics	1024x768	A0000	2/4/8	Both
56	16	128x48	8x16	Graphics	1024x768	A0000	4/8	Both
57	16	96x64	8x16	Graphics	768x1024	A0000	4/8	Both
58	16	160x64	8x16	Graphics	1280x1024	A0000	8	Interlaced
59	256	128x48	8x16	Graphics	1024x768	A0000	8	Interlaced
5A	32K	64x32	8x16	Graphics	512x512	A0000	4/8	Non-Interlaced
5B	32K	80x25	8x16	Graphics	640x400	A0000	4/8	Non-Interlaced
5C	32K	80x30	8x16	Graphics	640x480	A0000	8	Non-Interlaced

The Sync Specifications for Standard VGA Modes and Sync Specifications for Digital Monitors (EGA, CGA and Mono) are identical to those of the OTI-067.

OTI-077 EXTENDED REGISTERS

The OTI-077 provides extended registers identical to those of the OTI-067. In addition to these registers the OTI-077 provides support for the following new registers and enhancements to existing registers:

OTI OVERFLOW REGISTER II
SYSTEM SETUP REGISTER
VIDEO SUBSYSTEM ENABLE REGISTER

Descriptions of New Registers and Enhancements

94 SYSTEM SETUP REGISTER

This is a write only register. This register is effective only when the OTI-077 is in on-board configuration (3DFix12b2=1) and pin VSETUP(128) is a 0.

Bit	Description
0-4	Reserved
5	OTI-067 Enable/Setup. 0=OTI-067 in setup mode. Only write register 102 is allowed. 1=OTI-067 is in active mode. In active mode, access to OTI-067 is allowed only if bit 0 of register 102 is a 1, and either bit 0 of register 3C3 is a 1 or pin ENVGA (127) is a 1.
6	Reserved
7	System board Enable/Setup. This bit is not implemented.

3C3 VIDEO SUBSYSTEM ENABLE

This is a write only register. This register is effective only when the OTI-077 is in on-board configuration (3DFix12b2=1) and pin ENVGA(127) is a 0.

Bit	Description
0	OTI-067 Enable/Disable. 0=OTI-067 is disabled. No access to OTI-067 or OTI-077, video DAC (OTI-066) are allowed. 1=OTI-067 is enabled. Access to OTI-067 or OTI-077 are allowed only if bit 0 of register 102 is also a 1.
1-7	Reserved

Note: Access to this register is not effected by the state of register 102.

3DF OTI OVERFLOW REGISTER II INDEX 16

Bit	Description
0-2	Reserved
3	High Order Start Address Bit 9
4	High Order Cursor Location Bit 9
5	Page select for CRT display. This bit and bit 5 of the OTI OVERFLOW register (index 14) combine to select one of four 256K bytes of video memory.

3DFix16b5	3DFix4b5	256K byte page selected
0	0	First 256K bytes
0	1	Second 256K bytes
1	0	Third 256K bytes
1	1	Fourth 256K bytes

6 Page select for video memory accesses (both read and write). This bit and bit 6 of the OTI OVERFLOW register (index 14) combine to select one of four 256K bytes of video memory to be accessed.

3DFix16b5	3DFix4b5	256K byte page selected
0	0	First 256K bytes
0	1	Second 256K bytes
1	0	Third 256K bytes
1	1	Fourth 256K bytes

7 Test bit. This bit is used to mux in new video clock frequency during chip testing.

0=Internal pixel clock input is from pin VCLK (130).
1=Internal pixel clock is from pin VCLK if pin RA12 (64) is low and from pin RA13 (65) if pin RA12 is high.
Note that this bit active or pin RSET (106) active will turn pins RA12 & RA13 to input pins. However, while pin RSET has effect on pin RA14, this bit does not.

Note: Bits 6&5 should only be programmed if there exists 1Mega bytes of video memory. Programming these two bits when there are only 512K bytes of video memory may result in a blank display. Similarly, bits 6&5 of register 3DF index 14 should only be programmed if there exists 512K bytes of video memory.

Revised Registers and Bits

3DE EXTENSION REGISTER

Bit	Description
0-4	Same as OTI-067
5-7	ID bits.

Bit 7	Bit 6	Bit 5	Chip type
1	1	1	OTI-057, supports 256K memory only
0	1	0	OTI-067, supports 256K/512K memory only
1	0	1	OTI-077, supports 256K/512K/1MByte memory.

3DF OTI MISCELLANEOUS REGISTER INDEX D

Bit	Description
0-2	Same as OTI-067
3-4	extended graphics mode selection

Bit 4	Bit 3	Mode Selection
0	0	VGA modes and modes 4F, 50, 51, 52
0	1	High Resolution 256 colors(53,54, 1024x768 256)
1	0	1024x768 4 colors (55)
1	1	1024x768 16 colors (56)

5	Same as OTI-067
6-7	Memory configuration.

Bit 6	Bit 7	Mode Selection
0	0	256K memory available
0	1	512K memory available
1	0	Not supported
1	1	1 MByte memory available

These two pins are initially set to 01 at power up, then set to proper configuration by BIOS depending on how much memory is detected. Notice bit 6 can be used to turn off 1MByte support.

3DF SEGMENT REGISTER INDEX 11

Bit	Description
0-3	Read Segment for system memory read.
4-7	Write segment for system memory write.

Bit 3(7)	Bit 2(6)	Bit1(5)	Bit0(4)	Segment
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

In 640x480, 800x600, 1024x768 256 color modes, 1024x768 16 color mode, 768x1024 color mode, segmentation of the system address mapping to video memory is necessary to address all the pixel data. For these modes, the segment register should be used to access additional memory available.

3DF CONFIGURATION REGISTER INDEX 12

Bit	Description
0-2	Same as OTI-067
3	(CSEL0) OTI-077 functions enabled. Compatible with OTI-067 0=Same as OTI-067 1=Enables rev OTI-077 functions. Pin RDSWn becomes CAS2n, pin ROMENLn becomes ALE if bit 2 is also a 1.
4-5	Reserved
6-7	Same as OTI-067